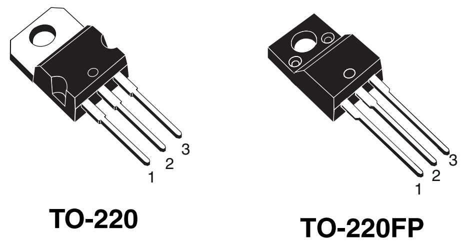
STP9NK65Z
STP9NK65ZFP

N-channel 650 V, 1 Ω, 6.4 A, TO-220, TO-220FP Zener-protected SuperMESH™ Power MOSFET

Features

Order codes	V_{DSS}	$R_{DS(on)}$ max.	I_D	Pw
STP9NK65Z	650 V	< 1.2 Ω	6.4 A	125 W
STP9NK65ZFP	650 V	< 1.2 Ω	6.4 A	30 W

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Extremely high dv/dt and avalanche capabilities



Applications

- Switching applications

Description

These devices are N-channel Zener-protected Power MOSFETs developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Figure 1. Internal schematic diagram

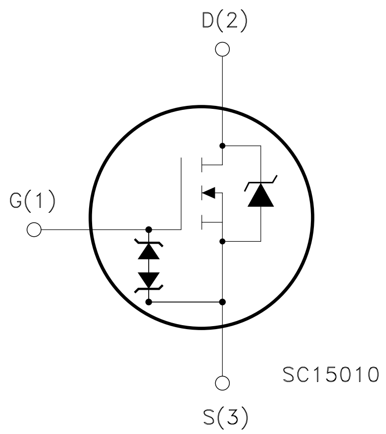


Table 1. Device summary

Order codes	Marking	Package	Packaging
STP9NK65Z	P9NK65Z	TO-220	Tube
STP9NK65ZFP	P9NK65ZFP	TO-220FP	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	650		V
V_{GS}	Gate- source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25 °C	6.4	6.4 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	4	4(1)	A
I_{DM} (2)	Drain current (pulsed)	25.6	25.6 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	125	30	W
	Derating factor	1	0.24	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100 pF, R=1.5 kΩ)	4000		V
dv/dt (3)	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (DC)	-	2500	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150 -55 to 150		°C °C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 6.4$ A, di/dt $\leq$ 200 A/µs, $V_{DD} \leq 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	1	4.2	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5		°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_{j\ max}$)	6.4	A
E_{AS}	Single pulse avalanche energy (starting T_j=25 °C, I_D=I_{AR}, V_{DD}=50 V)	200	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 650 V V_{DS} = 650 V, @125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 3.2 A		1	1.2	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 3.2 A	-	6	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	1145 130 28	-	pF pF pF
$C_{oss\ eq}$ (2).	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 400 V	-	55	-	pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 6.4 A, V_{GS} = 10 V (see *Figure 3*)	-	41 7.5 22	-	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 325 V, I_D = 3.2 A R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 2*)	-	20 12	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD} = 325 V, I_D = 3.2 A R_G = 4.7 Ω V_{GS} = 10 V (See *Figure 2*)	-	45 15	-	ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		6.4 25.6	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 6.4 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 6.4 A, di/dt = 100 A/µs V_{DD} = 50 V, T_j = 150 °C (see *Figure 4*)	-	400 2600 13		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 9. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}(1)	Gate-source breakdown voltage	Igs=±1 mA (open drain)	30	-	-	V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

3 Test circuits

Figure 2. Switching times test circuit for resistive load

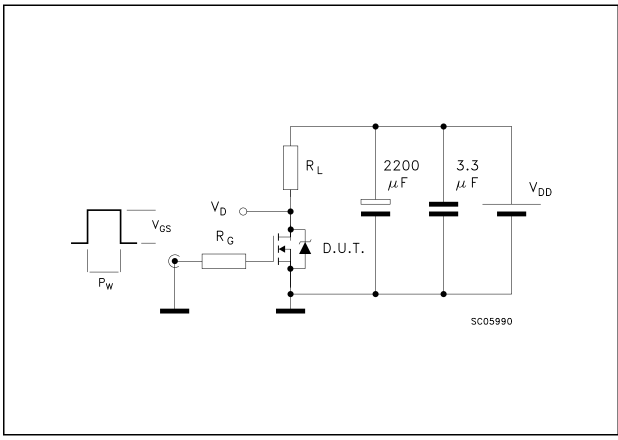


Figure 3. Gate charge test circuit

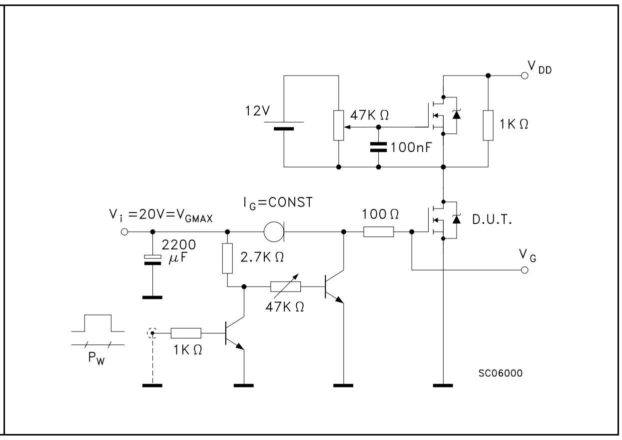


Figure 4. Test circuit for inductive load switching and diode recovery times

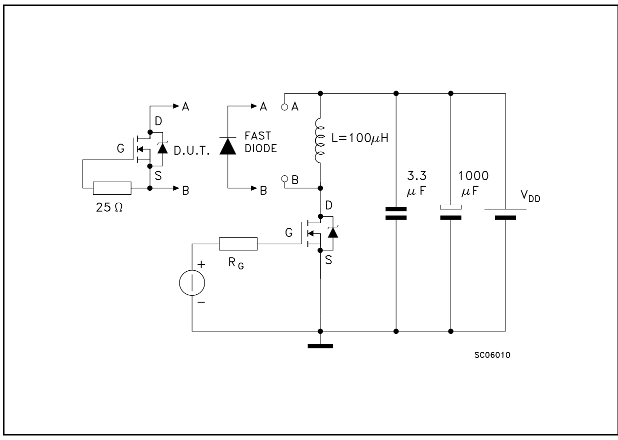


Figure 5. Unclamped Inductive load test circuit

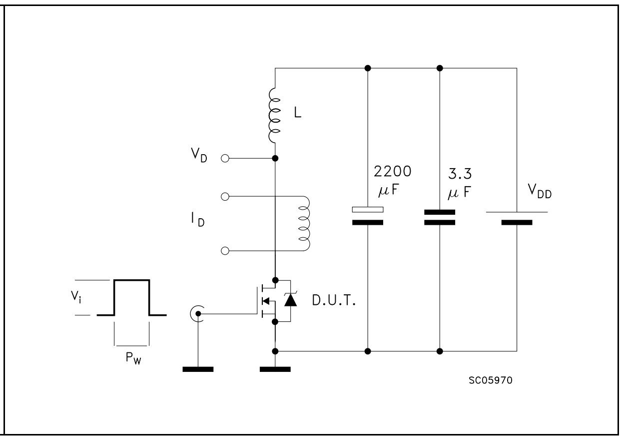


Figure 6. Unclamped inductive waveform

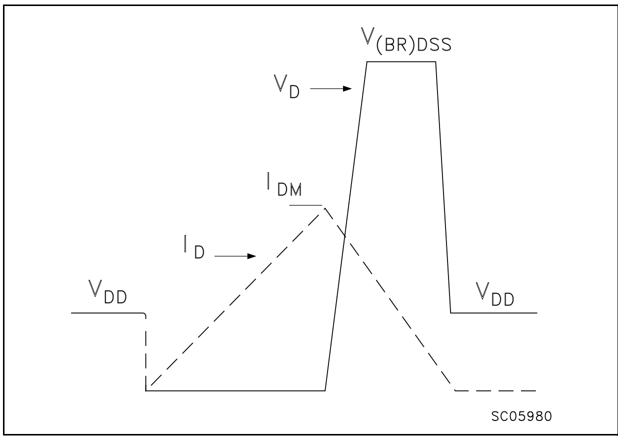
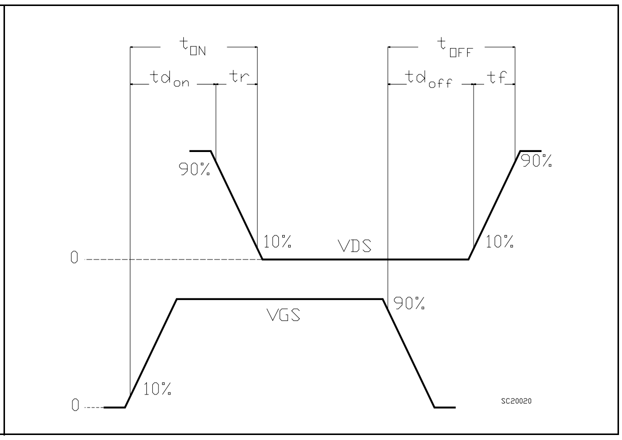


Figure 7. Switching time waveform



3.1 Electrical characteristics (curves)

Figure 8. Safe operating area for TO-220

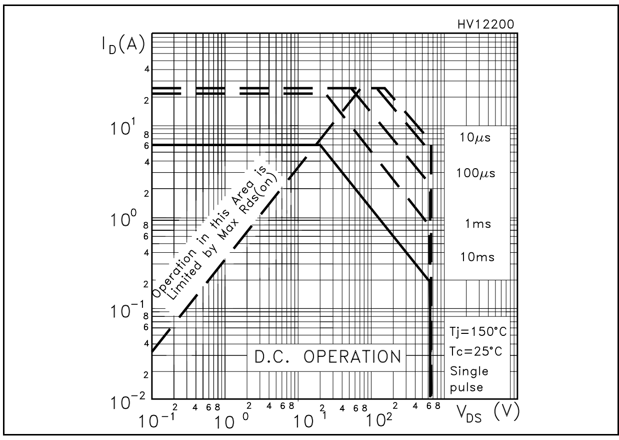


Figure 9. Thermal impedance for TO-220

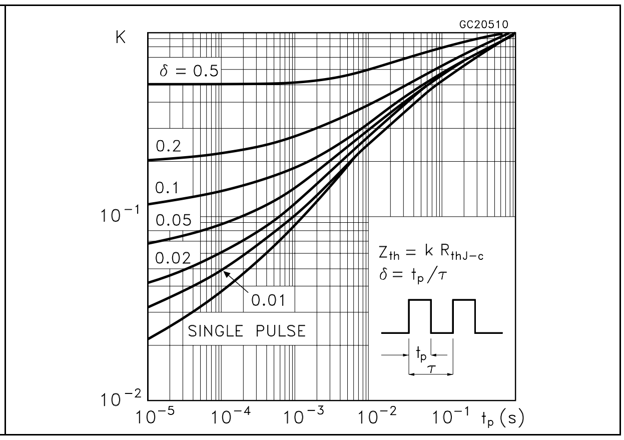


Figure 10. Safe operating area for TO-220FP

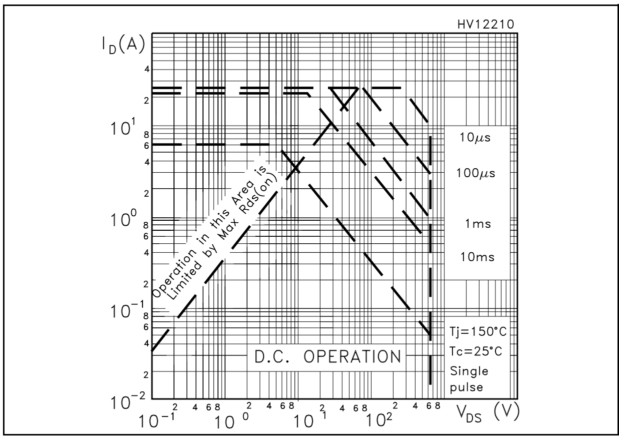


Figure 11. Thermal impedance for TO-220FP

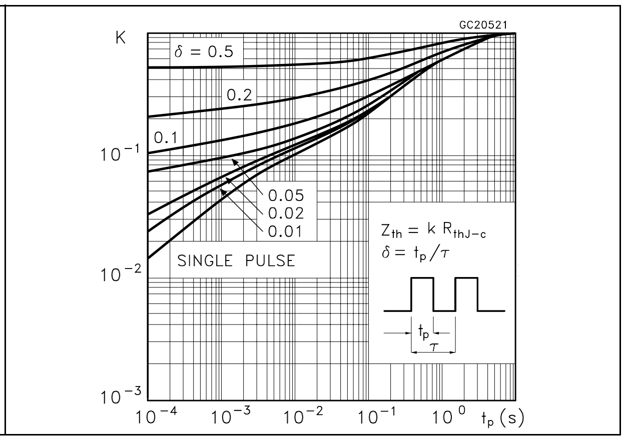


Figure 12. Output characteristics

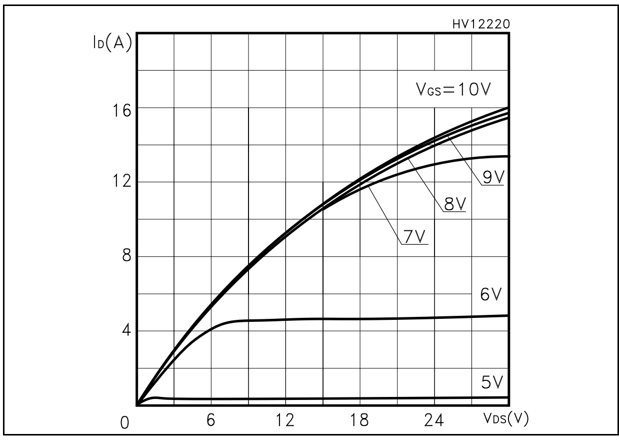


Figure 13. Transfer characteristics

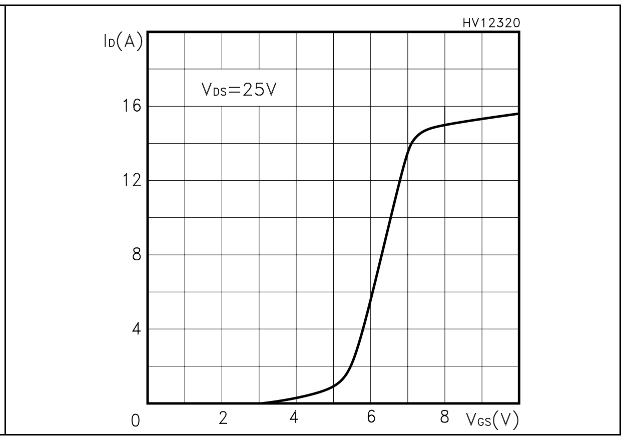


Figure 14. Transconductance

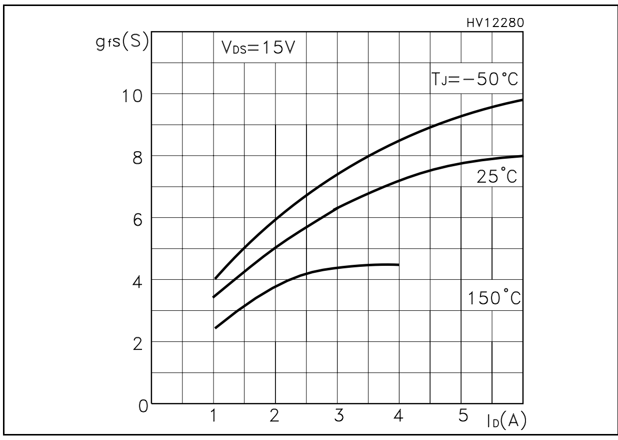


Figure 15. Static drain-source on resistance

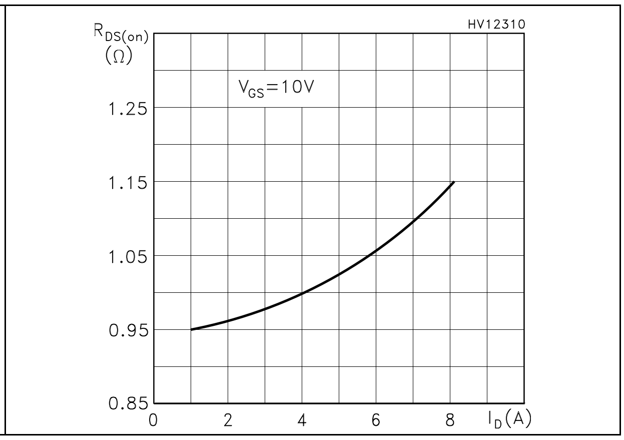


Figure 16. Gate charge vs gate-source voltage

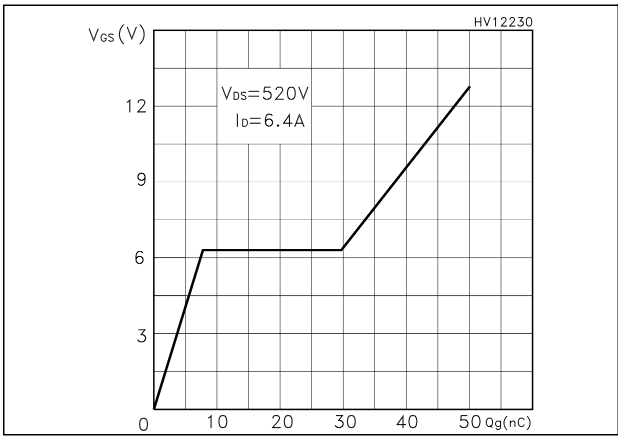


Figure 17. Capacitance variations

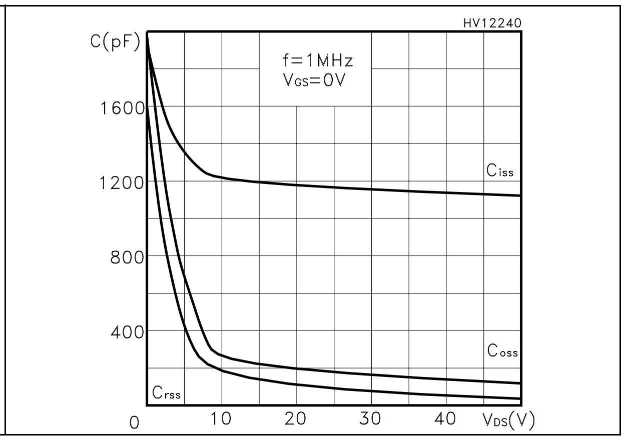


Figure 18. Normalized gate threshold voltage vs temperature

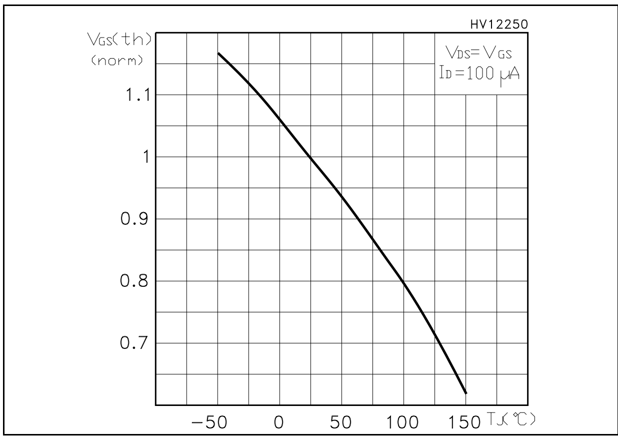


Figure 19. Normalized on resistance vs temperature

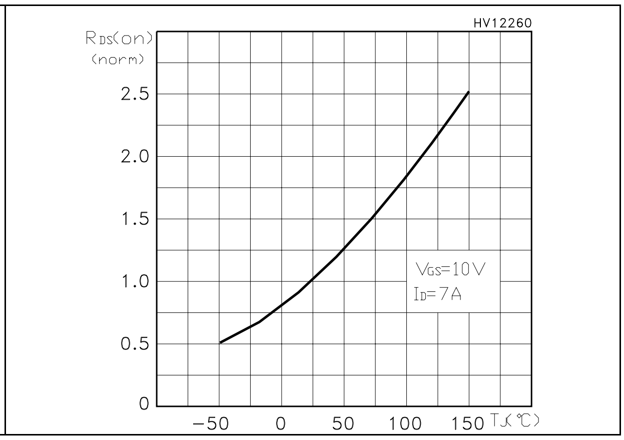


Figure 20. Source-drain diode forward characteristics

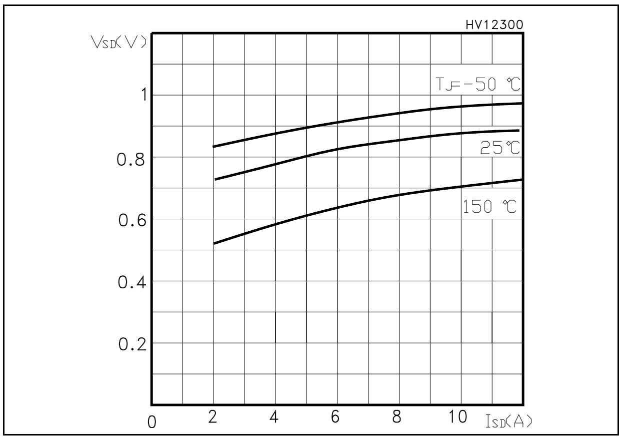


Figure 21. Normalized BV_{DSS} vs temperature

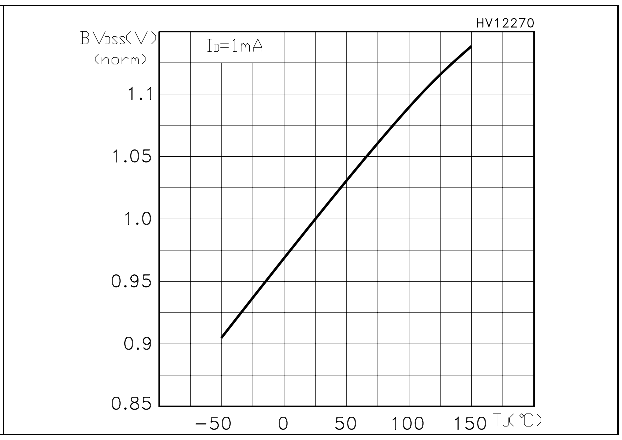
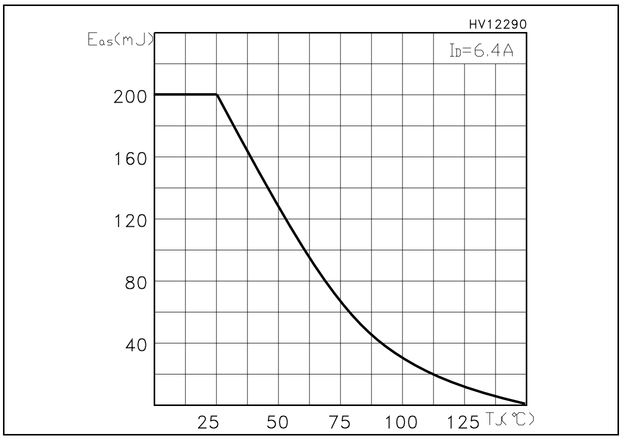


Figure 22. Maximum avalanche energy vs temperature



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 23. TO-220 type A drawing

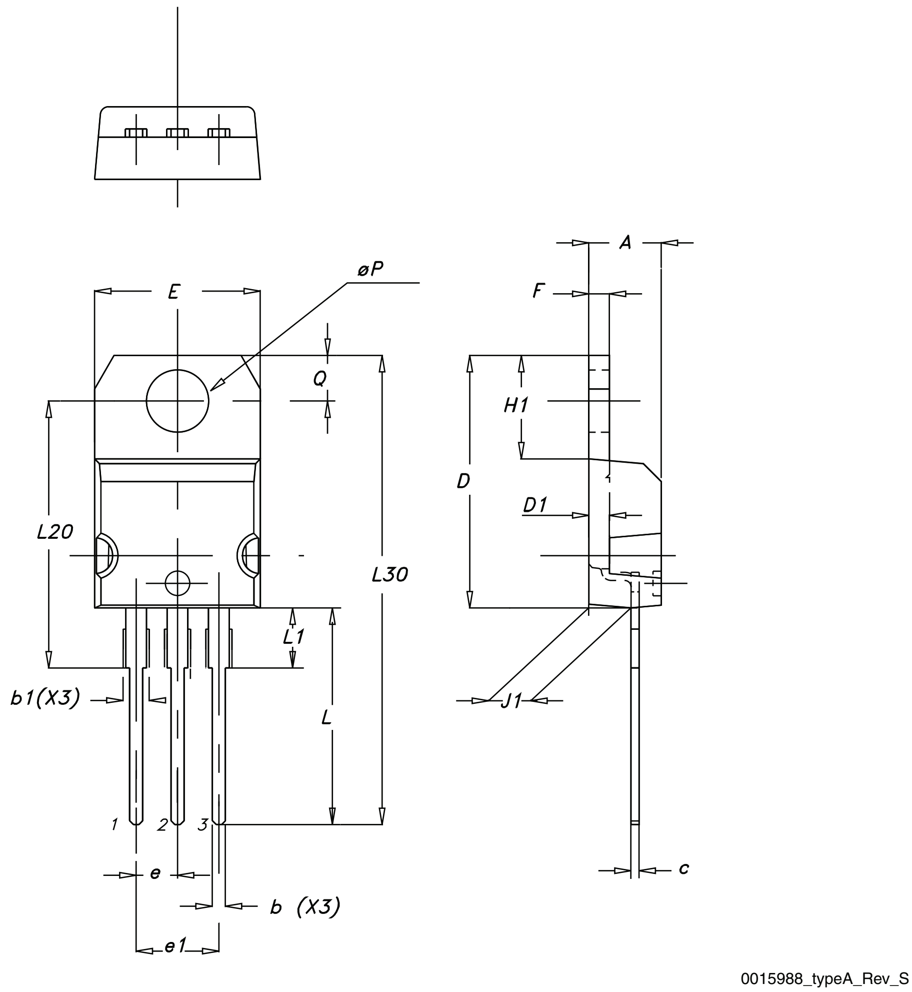
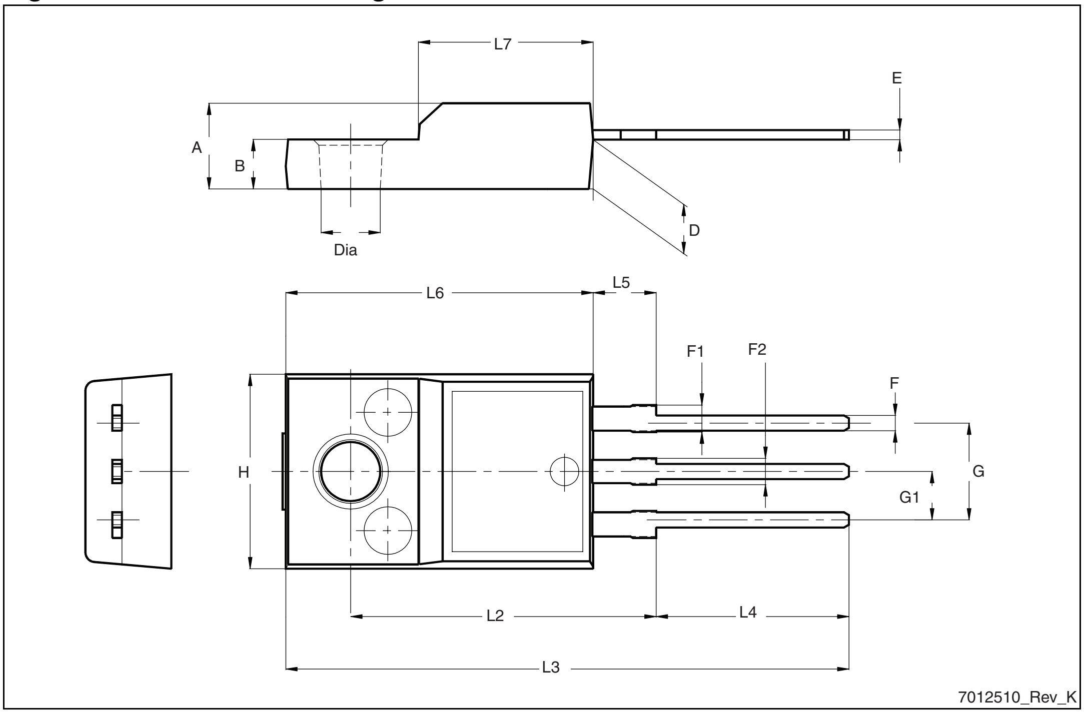


Table 11. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 24. TO-220FP drawing



5 Revision history

Table 12. Document revision history

Date	Revision	Changes
11-Sep-2006	2	Complete version
19-Dec-2007	3	The document has been reformatted
26-Jan-2012	4	– Minor text changes – Modified: *Features* in cover page – Updated: *Section 4: Package mechanical data*